IN THE CLAIMS:

Please cancel claims 37 and 38 as presented in the previous communication. Please add new claims 48-52.

48. (New) A system, comprising:

a memory; and

a processor coupled to the memory and to perform operations comprising:

executing an instruction that updates data in a register at a first time;

storing an instruction address of the instruction;

when the data is not read from the register at a next clock cycle from completion of execution of the instruction, setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and

when the instruction address of the instruction is encountered a second time and the bit indicates that the instruction is a slowable instruction, delaying processing of the instruction.

49. (New) The system of claim 48, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.

50. (New) The system of claim 48, wherein the processing of the instruction is delayed by delaying decoding the instruction.

51. (New) A system, comprising:

means for recording a first clock cycle when an instruction that loads data into a register is to complete;

means for storing an instruction address of the instruction;

means for recording a second clock cycle when the data is read from the register;

when the second clock cycle is more than one clock cycle from the first clock cycle, means for setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and

when the instruction address is encountered a next time, and the bit indicates that the instruction is the slowable instruction, means for delaying processing of the instruction.

52. (New) The system of claim 51, wherein the means for delaying the processing of the instruction comprises means for delaying decoding of the instruction.